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| 1. | Given the following memory values and a one-address machine with an accumulator ,what values do the following instructions load into the accumulator?   * Word 100 contains 300 * Word 200 contains 400 * Word 300 contains 500. * Word 400 contains 600.   a. LOAD IMMEDIATE 100  b. LOAD DIRECT 100  c. LOAD INDIRECT 100  d. LOAD IMMEDIATE 200  e. LOAD DIRECT 200  f. LOAD INDIRECT 200 |
| Soln. | 100 b) 300 c) 500 d) 200 e) 400 f) 600 |
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| 2. | Consider two processors P1 and P2 executing the same instruction set. Assume that under identical conditions, for the same input, a program running on P2 takes 25% less time but incurs 20% more CPI as compared to the program running on P1. If the clock frequency of P1 is 1GHz, then calculate the clock frequency of P2. |
| Soln |  |
| 3. | A processor accesses main memory with an average access time of T2. A smaller cache memory is interposed between the processor and main memory. The cache has a significantly faster access time of T1 << T2. The cache holds, at any time, copies of some main memory words and is designed so that the words more likely to be accessed in the near future are in the cache. Assume that the probability that the next word accessed by the processor is in the cache is H, known as the hit ratio.   1. For any single memory access, what is the theoretical speedup of accessing the word in the cache rather than in main memory? 2. Let T be the average access time. Express T as a function of T1, T2, and H.What is the overall speedup as a function of H?   In practice, a system may be designed so that the processor must first access the cache to determine if the word is in the cache and, if it is not, then access main memory, so that on a miss (opposite of a hit), memory access time is T1 T2. Express T as a function of T1, T2, and H.   1. Now calculate the speedup and compare to the result produced in part (b). |
| Soln. |  |
| 4. | The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB). The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards. Calculate the number of clock cycles required for the completion of execution of the sequence of all 100 instructions. |
| Soln. |  |
| 5. | Suppose that we are considering an enhancement that runs 10 times faster than the original machine, but is usable only 40% of the time. What is the overall speedup gained by incorporating the enhancement?  Solution:  N=10  f=40%    = 1.56 |
| 6. |  |

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